REMARKS/ARGUMENTS

Claims 2–6, 8–10, and 12–18 remain in the present application, of which claims 16, 17, and 18 are independent. Claims 8, 13, 16, and 17 are amended herein. Claims 1, 7, and 11 are cancelled. Applicants respectfully request reconsideration and allowance of claims 2–6, 8–10, and 12–18.

Claim Rejections under 35 USC § 102

Claims 2, 4–7, 9–10 and 12–18 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Hoberman (U.S. Patent Application Publication No. 2004/0268278).

In rejecting claim 18, on page 4 of the Office action, the Examiner appears to equate interface 265 of Hoberman FIG. 2 with the claimed interface island. Applicants respectfully traverse.

Independent claim 18 recites, in a relevant portion, "An integrated circuit, comprising: . . . a first computation island . . . a second computation island . . . an interface island for interfacing the first and second computation islands . . ." (Underlining added for emphasis.)

Hoberman, on the other hand, only discloses that "The low power standard cell logic block 262 and the low power memory block are coupled to an interface 265." See ¶ [0037]. Applicants submit that the interface 265 of Hoberman is not the same as an interface island, as claimed.

FIG. 2 schematically illustrates an embodiment of the invention including interface islands (the vertically hatched blocks) facilitating communication between computation islands (IP1–IP4). The interface island is defined in the specification, at least in ¶¶ [0043–44], referring to FIG. 2 and stating, "An island is composed of one or more IPs or modules that have common electrical and activity characteristics. This partitioning into islands can be obtained at the hardware/software co-design partitioning stage. A distinction between different types of islands is made: there are interface islands and computation islands. Computation islands are electrically independent, e.g. each island has a distinct power supply value Vdd, transistor threshold voltage Vt, and/or clock frequency ck. Two IP's belonging to the same island have the same Vdd-Vt-ck

triplet. Interface islands are aware of the distinct electrical characteristics of the various computation islands. . . Since each computation island can have unique electrical characteristics, they communicate to each other through the interface islands (hatched vertically). These interface islands take care of interfacing the distinctive electrical characteristics of the computation islands as to avoid data synchronization errors and signal integrity violations." (Underlining added for emphasis.)

Several features of exemplary embodiments of interface islands are also described at least in ¶ [0014], stating, "An interface island may comprise at least a voltage level shifting device to translate voltage levels from one computation island to another computation island. An interface island may furthermore comprise FIFOs for inter-island communications," and in ¶ [0047], stating, "The interface islands 39 between islands 30 may be implemented in any suitable manner, for example through FIFOS and using a technique called GALS (Globally asynchronous, locally synchronous). In this way, every island 30 is kept completely autonomous from the others."

Applicants submit that nowhere does Hoberman appear to disclose at least one interface island for interfacing at least two of the plurality of computation islands. To anticipate a claim, however, the reference must teach every element of the claim. In other words, all claim elements, and their limitations, must be found in the prior art reference to maintain a rejection based on 35 U.S.C. § 102. Therefore, Hoberman must disclose all limitations of claim 18 for the anticipation rejection of independent claim 18 to be sustained. For at least these reasons, Applicants respectfully request the rejection of claim 18 be withdrawn and that this claim be allowed.

Independent claim 16 has been amended to substantially incorporate the limitations of former dependent claim 7.

Claim 16 as amended now recites in a relevant portion: "An integrated circuit, comprising: a plurality of computation islands . . . and at least one interface island for interfacing at least two of the plurality of computation islands . . ." (Underlining added for emphasis.)

For at least reasons that are substantially the same as those given above in reference to claim 18, Hoberman does not disclose the above limitation of claim 16. Therefore, claim 16 was not anticipated by the Hoberman reference. Therefore, Applicants request that the rejection of claim 16 be withdrawn and that this claim be allowed.

Independent claim 17 has been amended to incorporate a portion of former dependent claim 13.

Claim 17 as amended now recites in a relevant portion, "A method for real-time tuning of at least one utility value of an integrated circuit . . . the method comprising: monitoring at least one working parameter related to a working condition of the integrated circuit; . . . wherein the at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, or logic noise margin values." (Underlining added for emphasis.)

Applicants submit that nowhere does Hoberman appear to disclose wherein the at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, or logic noise margin values. For at least this reason, claim 17 as amended was not anticipated by Hoberman. Therefore, Applicants request that the rejection of claim 17 be withdrawn and that this claim be allowed.

Because claims 2, 4–6, and 9–10 depend, directly or indirectly, from claim 16, and claims 12–15 depend, directly or indirectly, from claim 17, they each incorporate all the terms and limitations of claims 16 and 17, respectively, in addition to other limitations, which together further patentably distinguish these claims over the art of record. Therefore, Applicants request that the rejection of claims 2, 4–6, 9–10, and 12–15 be withdrawn and that these claims be allowed.

Claim Rejections under 35 USC § 103

Claims 3 and 8 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hoberman (U.S. Patent Application Publication No. 2004/0268278) in view of Chandrakasan (U.S. Patent Application Publication No. (2004/0183588).

Chandrakasan appears to have been cited only for its alleged disclosure of the adjusting of the threshold voltage of a transistor by controlling a bulk voltage, and for its alleged disclosure of the use of a triple-well CMOS technology. Nowhere does Chandrakasan appear to disclose, teach, or suggest the use of interface islands for interfacing at least two of the plurality of computation islands as claimed in claims 18 and 16, nor does it appear to disclose, teach, or suggest a method where at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, or logic noise margin values, as claimed in claim 17.

Thus, Chandrakasan does not supply the deficiencies of Hoberman, so there is no apparent reason why a person having ordinary skill in the art would have combined the teachings of the cited references to arrive at an embodiment of the claimed invention. Therefore, Applicants request that the rejection of claims 3 and 8 be withdrawn and that these claims be allowed.

Concluding Remarks

In view of the foregoing amendments and remarks, Applicants earnestly solicit a timely issuance of a Notice of Allowance with claims 2–6, 8–10, and 12–18. If there are any remaining issues that can be addressed over the telephone, the Examiner is cordially invited to call Applicants' attorney at the number listed below.

Respectfully submitted,
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626/795-9900

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